A 55.0 Gb/s/cm data bandwidth density interface in 0.5 μm CMOS for advanced parallel optical interconnects

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Abstract

We demonstrate that low-cost 0.5μm CMOS may be used to bridge between a slow parallel electrical interface and a very high-speed parallel optical interface. The 1 cm-wide integrated circuit has a bisection data bandwidth of 55 Gb/s and dissipates 5.7 W.

INRODUCTION

Edge-connector bandwidth density (Gb/s/cm) is a known barrier to efficient system integration [1]. A promising solution exploits the inherently high-bandwidth density of ribbon-fiber based parallel optical interconnects. The industry standard MT fiber connector uses an approximately 6 mm wide ferrule which holds 12 multi-mode glass fibers on a 250 μm pitch. Hence, an optoelectronic transceiver port with 12 transmit and 12 receive fibers is best accommodated using a sub-12 mm wide (< 2 x 6 mm) electronic interface. The challenge for CMOS is to deliver the needed bandwidth density to the optoelectronic interface while at the same time effectively bridging to the lower bandwidth density of conventional CMOS electronics. The purpose of this letter is to demonstrate that low-cost 0.5 μm CMOS is capable of providing a multiplexed 55 Gb/s/cm interface. This edge-connector bandwidth density is a factor of 10 greater than the competing state-of-the-art HIPPI-6400 parallel electrical interconnect [2].

RESULTS

A functional block diagram of the circuit is shown in Figure 1 (a). Each of the twelve transmit (Tx) and twelve receive (Rx) high-speed signal lines of the 2:1 / 1:2 multiplexer (MUX) Integrated Circuit (IC) sustains a data rate of 2.5 Gb/s without errors. The IC dissipates 5.7 W from a 3.6 V power supply, of which 0.225 W is for the high-speed side parallel load termination and 1.025 W for the source and load terminated Low Voltage Differential Signalling (LVDS) [3] compatible slow-speed side. The Tx part of the IC receives a full-speed clock (Clk2) running at twice the slow-speed input data rate. This clock can be delayed to ensure all input data lines latch successfully. An additional delay circuit is provided for the high-speed clock output path so that the receive side clk-data setup times (hold time is zero on the high-speed input flip-flops) can be satisfied across all the channels. The measured delay range is in excess of 400 ps (1 ns) at 2.5 Gb/s (1.25 Gb/s) at the high-speed output without exercising the 0°/180° phase selection circuit, which effectively doubles the range. The measured jitter of the high-speed clk output referenced to the input has a minimum value of 3.77 ps rms (26.2 ps peak-to-peak) increasing to 4.25 ps rms (27.2 ps peak-to-peak) and 6.62 ps rms (46.4 ps peak-to-peak) at the extreme delay settings. The significant increase in jitter at one end of the range is due to the increased contribution of the inherent switching-threshold uncertainty of the cross-coupled pair in the delay elements.

Figure 1 (b) shows a photograph of the 10.3 x 2.33 mm^2 IC. Signals are launched onto the test fixture Printed Circuit Board (PCB) using RG178 3M cables [4] with 0.1" pitch jumper stakes as connectors. Small signal insertion loss measurements of the electrical loop-back path which includes 24" of RG178 3M cable, jumper stake connectors, representative PCB trace, and IC package routing indicate a -6 dB response at 1.25 GHz. To compensate, the IC uses receive and transmit circuits with peaking [5] by insertion of a zero in the differential amplifier load. The receive-transmit circuit cascade has a measured -3 dB bandwidth of 1.7 GHz, corresponding to error-free 3.3 Gb/s performance. A differential amplifier with a level-shifted output stage and active pull-down is used as the clock buffer on the IC. This approach exhibits relatively low sensitivity to capacitive loading.

Figure 2 shows the measured phase margin of the high-speed output side of the IC at 2.5 Gb/s (400 ps bit period) with insets showing a representative electrical and optical eye-diagram and sensitivity of the high-speed input side of the 12 wide Tx-Rx path in electrical loop-back on the slow-speed side. Electrical measurements are performed with a 2^{31} -1 Non-Return to Zero Pseudo-Random Bit Stream (NRZ PRBS) at an input data amplitude of 126.5 mVpp. Diamonds and squares correspond to best-case and worst-case signal lines respectively among the 12-wide high-speed data input interface. The measured worst case phase margin is better than 210 ps at 2.5 Gb/s at a Bit Error Ratio (BER) of 10^{-12} and the electrical sensitivity is better than 130 mVpp at a BER of 10^{-12}.

Figure 3 shows the measured phase margin of the slow-speed output side at 1.25 Gb/s (800 ps bit-period) with insets showing a composite eye-diagram of all 22 positive data outputs and sensitivity of the slow-speed input side of the 22-wide Tx-Rx data path in electrical loop-back. Squares and diamonds correspond to best-case and worst-case signal lines respectively among the 22-wide slow-speed data input interface. Input data amplitude is 125 mVpp with a common-mode of 1.2 V. The worst-case phase margin is better than 510 ps at 1.25 Gb/s and a BER of 10^{-12}. The measured electrical sensitivity is better than 80 mVpp at 10^{-13} BER.

Worst-case measured crosstalk from adjacent high-speed output lines (including IC-package,

PCB, and connectors) is -20.3 dB (pp). The measured jitter on the high-speed data outputs referenced to the input is between 9.1 ps rms (64 ps peak-to-peak) and 16.3 ps (99 ps peak-to-peak). The measured jitter on the slow-speed data outputs measured in electrical loop-back on the high-speed side) is between 9.1 ps rms (58 ps peak-to-peak) and 22.14 ps rms (116 ps peak-to-peak). The combined Tx / Rx end-to-end link latency of the MUX IC at 2.5 Gb/s signalling rate is measured to be 2.7 ns.

CONCLUSION

Low-cost 0.5 μm CMOS is capable of providing the needed performance and functionality to bridge from a slow-parallel electronic interface to the very high edge-connector bandwidth density of advanced parallel optical interconnects. Such optoelectronic ports will be used to remove edge-connector system integration bottlenecks.

ACKNOWLEDGEMENTS

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References:

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[2] 'High-performance parallel interface - 6400 Mbit/s physical layer (HIPPI-6400-PH)', Tech. Committee of Accredited Standards, X3T11, May 1996.

[3] 'Draft Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)' (IEEE, New York, 1992), Draft 1.26 IEEE P1596.3-1995.

[4] 3M part number 982424-017-XXX

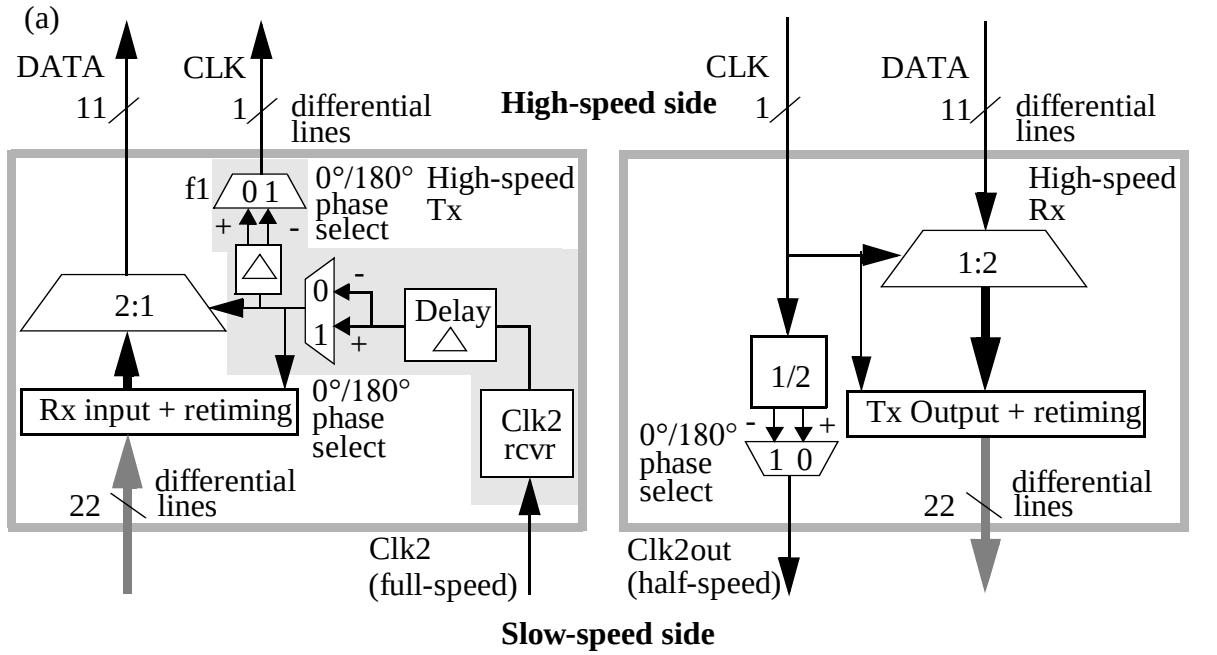
[5] MADHAVAN, B., and LEVI, A. F. J.: 'Low Power 2.5 Gb/s VCSEL driver in 0.5 μm CMOS technology', Electronics Letters, 1998, **34**, pp 178-179.

Figures:

Figure 1: (a) Functional block diagram of 2:1 / 1:2 mux / demux IC. The slow-speed side with 22-data and 1-clock LVDS signal lines and high-speed side with 11-data and 1-clock differential signal lines is indicated. (b) Photograph of MUX IC measuring 10.3 mm x 2.3 mm.

Figure 2: Measured high-speed side (2.5 Gb/s, 400 ps bit-period) phase margin with electrical loop-back on the slow-speed side (1.25 Gb/s) and 126.5 mVpp differential input data amplitude. Diamonds are best-case and squares are worst-case signal line. Insets are representative electrical and optical eye-diagram of high-speed 2.5 Gb/s output (vertical scale is 200 mV/div and the horizontal scale is 100 ps/div). Also shown is the measured high-speed side (2.5 Gb/s) input sensitivity with electrical loop-back on the slow-speed side (1.25 Gb/s). The optical eye-diagram is obtained using the MUX IC output to drive an oxide-confined Vertical Cavity Surface Emitting Laser (VCSEL) diode.

Figure 3: Measured slow-speed side (1.25 Gb/s, 800 ps bit-period) phase margin with electrical loop-back on the high-speed side (2.5 Gb/s) and 125 mVpp differential input data amplitude. Diamonds are best-case and squares are worst-case signal line. Insets are composite eye-diagram of 22 superimposed positive slow-speed 1.25 Gb/s outputs (vertical scale is 50 mV/div and the horizontal scale is 200 ps/div) and the measured slow-speed side (1.25 Gb/s) input sensitivity with electrical loop-back on the high-speed side (2.5 Gb/s).


(a)
DATA
11
CLK
1
differential lines
High-speed side
CLK
1
DATA
11
differential lines
f1
0 1
0°/180° phase select
High-speed Tx
+
-
2:1
0
1
-
+
Delay
Rx input + retiming
0°/180° phase select
Clk2 rcvr
22
differential lines
Clk2 (full-speed)
High-speed Rx
1:2
1/2
0°/180° phase select
- +
1 0
Tx Output + retiming
22
differential lines
Clk2out (half-speed)
Slow-speed side

(b)

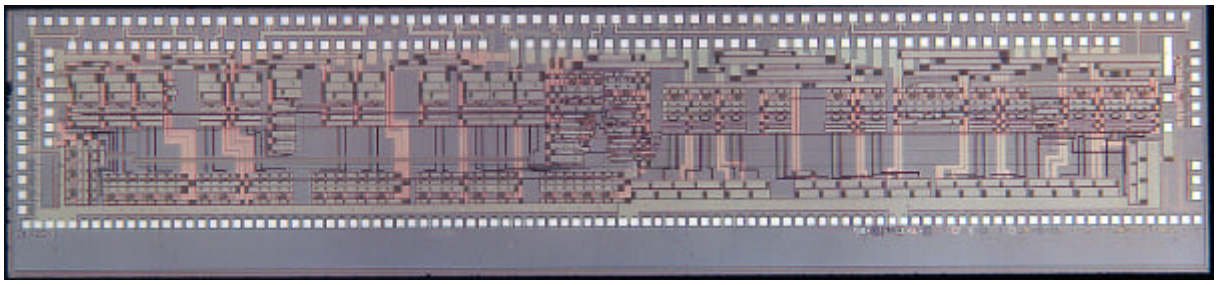


Figure 1

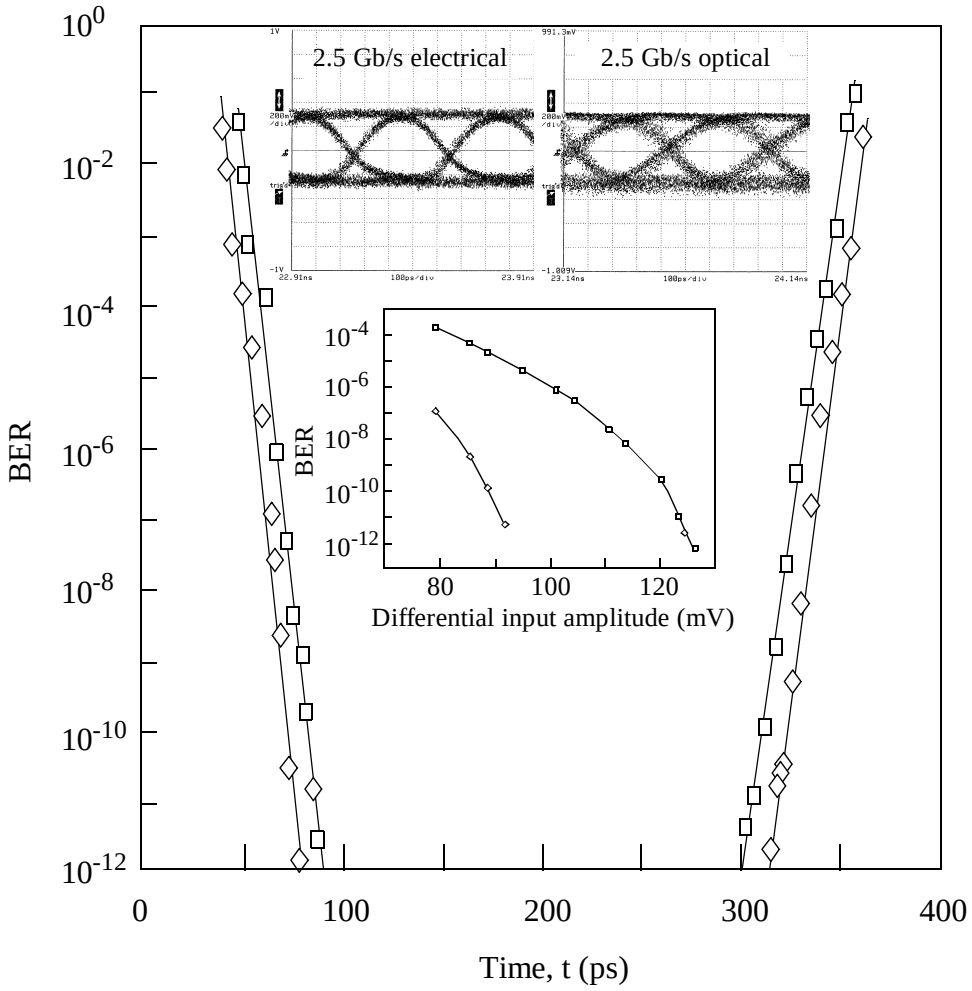

2.5 Gb/s electrical
2.5 Gb/s optical
BER
Time, t (ps)
Differential input amplitude (mV)

Figure 2

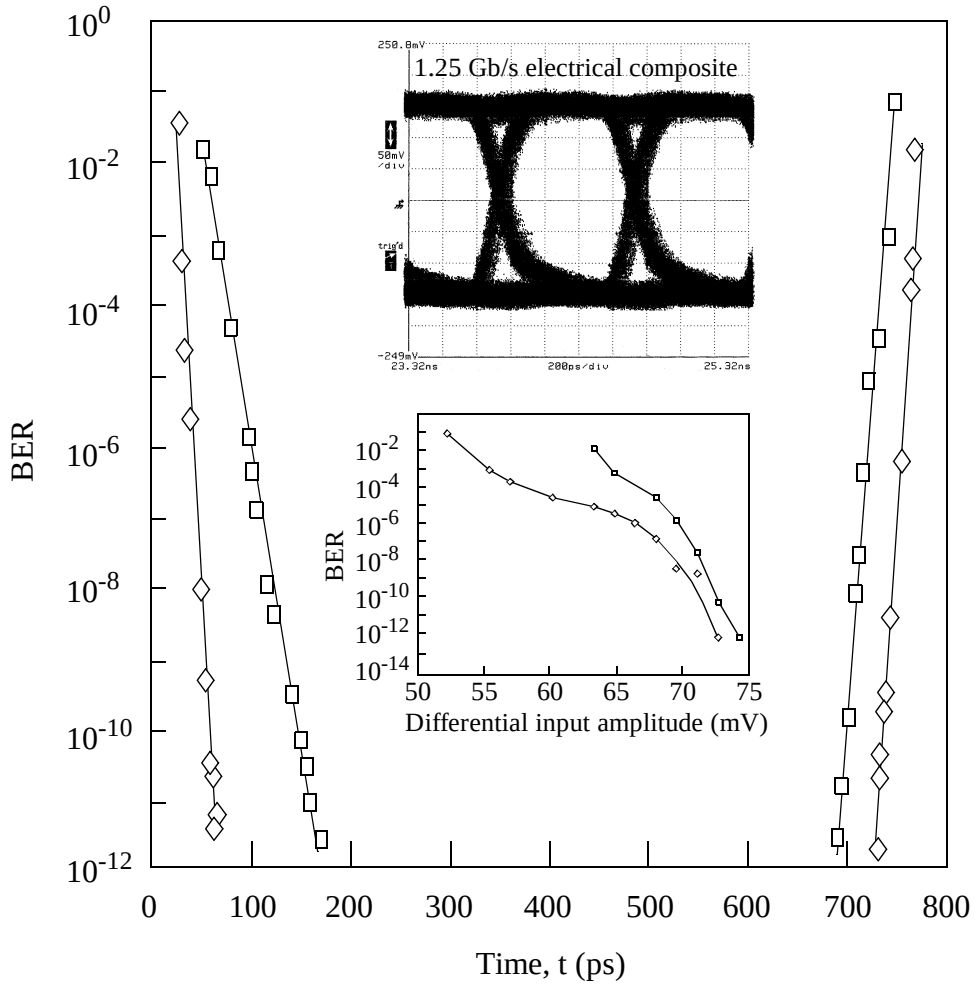

1.25 Gb/s electrical composite
250.0mV
50mV /div
-249mV
23.32ns
200ps/div
25.32ns
BER
Differential input amplitude (mV)
Time, t (ps)

Figure 3