# 622 Mb/s/Channel Parallel Digital Optical Receiver Array Module Using Hybrid Packaging

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***Abstract*—Given the high data rates (>500 Mb/s) achievable in optical links using current device technologies, low cost packaging of transmitters and receivers plays a key role in rendering them viable for short-haul data communication networks. The authors report a 12 channel, fully digital, hybrid receiver module for a synchronous parallel optical datalink operating at 622 Mb/s/channel. The use of a multichip module (MCM) and the passive alignment of the MT-connectorized multimode ribbon fiber to the photodetector array result in a simple low cost packaging solution.**

***Index Terms*—Optical communication, optical receiver, parallel link, hybrid receiver.**

## I. Introduction

ADVANCES in device technologies and computer architectures are drastically improving the computing speeds of processors, necessitating the development of interconnections with low latencies and throughputs in the Gb/s regime to tap the vast potential of distributed computing [1] and the advantages of integration of data from diverse sources. Short-haul (10–500 m) parallel optical links have been identified as a means of meeting the growing demand for high data-rates on networks [2]–[7]. However, while long-haul telecommunication links can tolerate a high cost/bit ratio, cost and ease of installation are very important issues that need to be addressed in order to provide a viable alternative to existing copper links in short-haul data networks. Optical fiber interconnections for high-capacity multiple channel applications can be realized either by serial links based on time-division multiplexing (TDM) techniques or parallel links. Serial implementation of high-aggregate data rates (several Gb/s) using a single optical channel would necessitate the use of expensive components for data transmission, reception, clock recovery, retiming, and multiplexing/demultiplexing. Thus, the serial approach may lead to potentially higher cost compared with parallel links which employs low cost 1 Gb/s technology and extend it to a number of channels. Recently, considerable effort has been focused on cost-effective means of packaging optical communication chips and innovative methods of coupling light from transmitters to photodetector arrays [6]–[9]. We report a packaging strategy for a 12 × 622 Mb/s parallel synchronous optical link utilizing volume manufacturable parts and a passive fiber-photodetector alignment technique.

The paper is organized as follows: In Section II, we describe the receiver array design and outline packaging requirements warranted by crosstalk considerations. Package design of the receiver module is described in Section III. Test results of the receiver array are presented in Section IV. The scope for future work is described in Section V and our conclusions are drawn in Section VI.

## II. Receiver Array Design

Computer communication applications place stringent requirements on the performance characteristics of short-haul synchronous parallel optical links, which include i) very low bit-error rates (BER $< 10^{-14}$), ii) low interchannel interference or crosstalk (less than −40 dB), iii) small interchannel skew (<10 ps/m), iv) dc coupling to permit transparent data transfer and bursty traffic, v) low system power dissipation (<100 mW/channel), vi) high data transfer rate per channel (>500 Mb/s), vii) ease of packaging and assembly, and viii) low cost. By applying multiple critical technologies, a receiver array module comprised of 12 (10 data and 2 clock) channels was designed to meet these requirements [10]. The array may be used to build a byte-wide link with two parallel channels for supervisory and/or error detection/correction (EDC) data. A schematic outline of the receiver array is depicted in Fig. 1. The optical signals are input via a graded-index multimode (MM) optical ribbon fiber to a p-i-n photodiode array. Two of the input channels (Channels 5 & 11) carry the transmitted clock signal and the remaining are data channels. The transmitted clocks enable synchronous data regeneration without the need for clock-recovery circuitry. The photocurrents from the p-i-n photodiodes are amplified by a front end amplifier array. The data outputs of the amplifiers are then retimed by a commercially available bipolar transistor D flip-flop array clocked by the amplified clock signals. A complete decision circuit with an input comparator is not employed for the purpose of keeping the power dissipation low.

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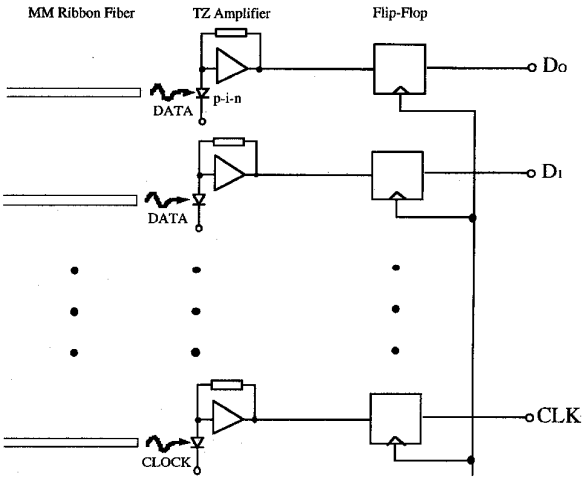


Fig. 1. Schematic illustration of optical receiver array.

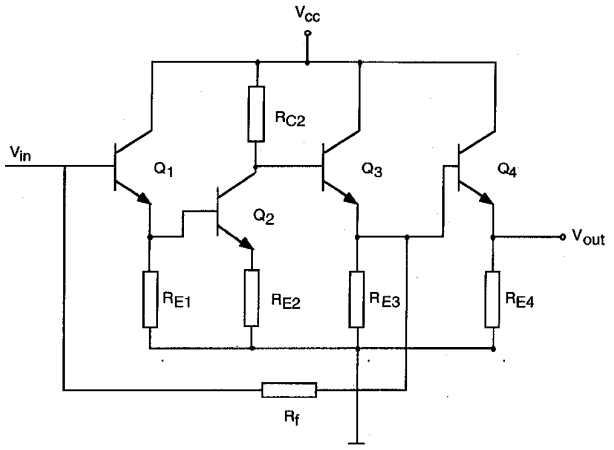


Fig. 2. Circuit diagram of the single-channel transimpedance amplifier ($R_f$ = 2 kΩ).

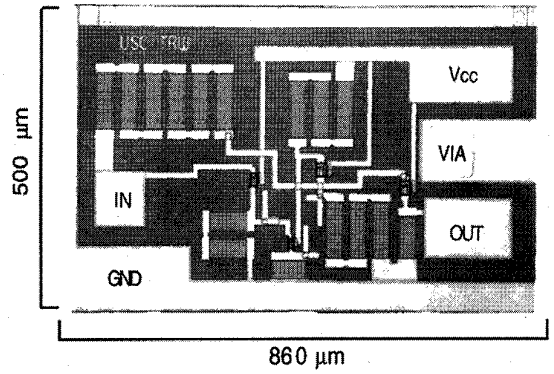


Fig. 3. Photomicrograph of a single channel transimpedance amplifier chip.

The receiver system described in this paper envisages the use of transmitter arrays that provide optical signal swings in excess of −5 dBm. Such optical signal swings have been routinely achieved using laser diode transmitters at bit-rates >1 Gb/s. Recently, low-threshold three-terminal laser diodes have been demonstrated to provide power-efficient, dc-coupled, large-signal on–off digital modulation at Gb/s bit-rates and low BER [11]. The relatively large switched optical power, coupled with the low attenuation of silica optical fibers over the distances targeted in short-haul links, allows us to restrict the front-end to a single stage transimpedance amplifier array (TIAA) whose output signals can directly drive the inputs of the decision circuits, thereby reducing power consumption.

The receiver utilizes a 12-channel TIAA fabricated in the TRW self-aligned base metal (SABM) AlGaAs/GaAs heterojunction bipolar transistor (HBT) foundry process [12]. The transistors used were of emitter size 3 $\mu$m × 10 $\mu$m, with $f_T$ > 25 GHz and $f_{\max}$ > 35 GHz at an emitter current density of 10 kA/cm$^2$. The circuit diagram of the unit cell is shown in Fig. 2. The feedback resistance $R_f$ is 2 kΩ, and the output of the amplifier is designed to drive a dc coupled 50 Ω load. The ability to provide a low-inductance ground connection to the chip is of paramount importance in the design of high gain-bandwidth product amplifiers. The ground connection was made to the metallized backside of our chip using a substrate through-hole via, a feature available in the foundry technology on the semi-insulating GaAs substrate. Fig. 3 shows a photomicrograph of a single-channel amplifier chip which measures 860 $\mu$m × 500 $\mu$m. The dual-loop feedback transimpedance amplifier has a measured transimpedance gain of 65 dBΩ over a 3-dB bandwidth of 2.3 GHz with a $V_{cc}$ = +5 V. The Gaussian-noise limited sensitivity of the amplifier is −26.5 dBm [13]. The array exhibits excellent uniformity in the performance characteristics.

Data retiming of the TIAA outputs is realized using two 6-b ECL D-register chips with single-ended inputs and differential outputs commercially available from Motorola [14]. The register chips operate up to a clock frequency of 622 MHz.

## III. Package Design

The detector stage consists of a custom 16-wide top-illuminated $In_{0.53}Ga_{0.47}As$ common cathode p-i-n photodiode array with center-to-center spacing of 250 $\mu$m [15]. Each photodiode has a capacitance less than 350 fF at a reverse-bias voltage of 3 V and a responsivity of 0.7 A/W at a wavelength of 980 nm. A recess in a precision-machined stainless-steel block enables passive alignment of the photodiode array to the fiber ribbon by means of the guiding pins of an MT fiber array connector [16] as illustrated in Fig. 4. Given that the diameters of the p-i-n photodiode active area and of the multimode (MM) fiber core are 80 $\mu$m and 62.5 $\mu$m, respectively, the tolerance in machining this block can be as large as 20 $\mu$m without sacrificing more than 3 dB in the coupling efficiency from the ribbon fiber. The photodiode mounting block is the only high-precision part in the module, making this a potentially low-cost packaging solution.

Because the center-to-center spacing in the p-i-n photodiode array and the TIAA array are 250 $\mu$m and 500 $\mu$m, respectively, an electrical fanout section from the p-i-n array had to be utilized. It consists of a patterned ceramic substrate which

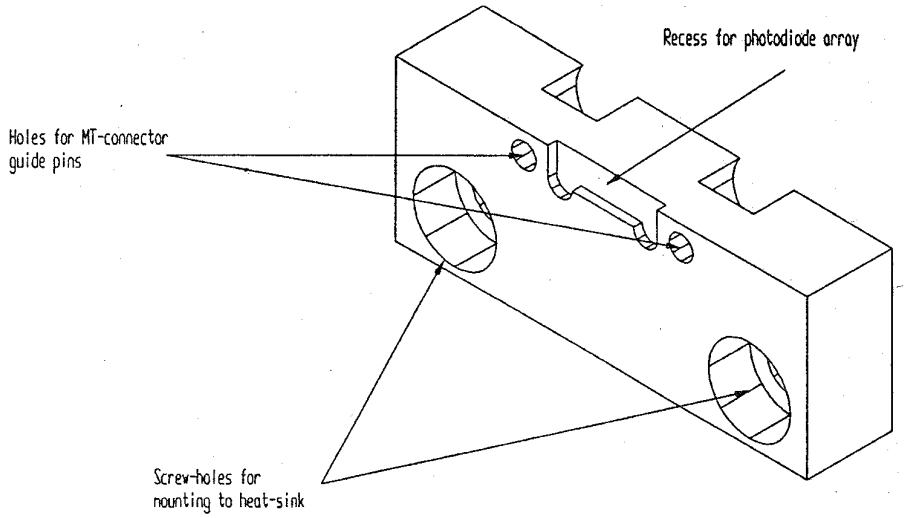


Fig. 4. Illustration of precision-machined stainless steel block with recess for photodiode array and holes for MT-connector guide pins.

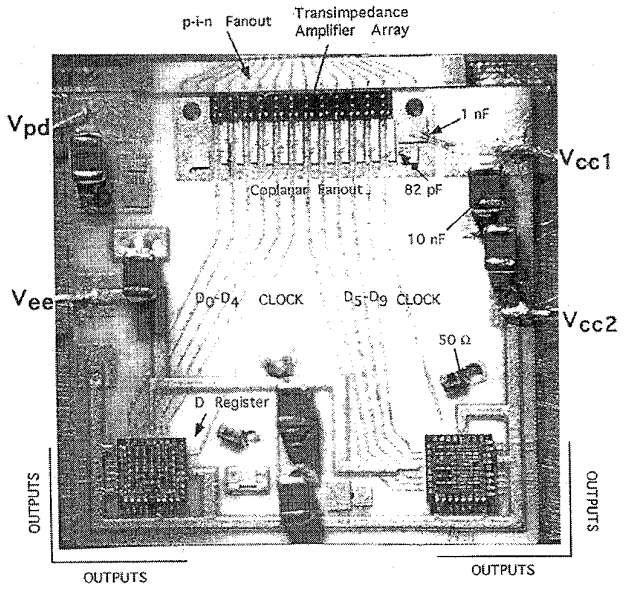


Fig. 5. Photograph of the 12-channel receiver array MCM.

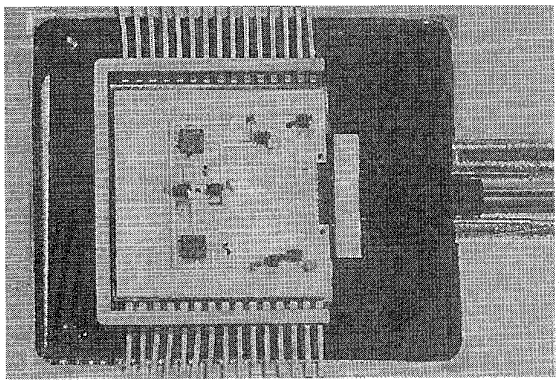

Fig. 6. Photograph of MCM and photodiode subassembly mounted in the leadframe package.

is soldered on the top side of the gold-plated stainless-steel block. The fanout lines are wrapped around one edge of the substrate, thus making wire-bonding to the photodiode array a simple task.

The p-i-n fanout lines were wire-bonded to the input pads of the TIAA chip, which is packaged in a multichip module (MCM). A detailed photograph of the completed MCM is shown in Fig. 5. The MCM substrate consists of a two-layer thick-film hybrid. The TIAA chip was attached to ground metallization on the ceramic motherboard using conductive epoxy. The outputs of the TIAA were wire-bonded to an array of coplanar lines which fanned out into microstrip lines to the two D-register chips. Plated-thru ground vias throughout the coplanar section provide excellent ground connection. The ground metallization of the coplanar lines allowed an 82 pF single-layer chip capacitor to be provided close to each amplifier cell to bypass the power rail ($V_{cc1} = +5$ V). In addition to the 82 pF capacitors attached close to the TIAA chip, 1 nF single-layer and 10 nF multilayer capacitors were also provided for decoupling the supply lines [17]. Two power supplies ($V_{ee}$ and $V_{cc2}$) had to be used to render the input dc levels of the decision circuits compatible with the output bias voltages of the transimpedance amplifier for dc coupling the analog and digital circuits. The ten retimed outputs were wire-bonded to 50 Ω microstrip transmission lines which fanned out to the leads of a leadframe package into which the MCM is soldered. This is shown in Fig. 6. The inside of the leadframe package measures 21 mm × 21 mm.

The assembly process involves attaching the photodiode block to a gold-plated copper heat sink (Fig. 7) which is preattached to the leadframe package. The resulting part is sealed inside a two-piece plastic-molded carrier. The overall dimensions of the completed module are 37.5 mm × 31 mm × 4.5 mm.

## IV. Results

A photograph of the evaluation board used to test our receiver module is shown in Fig. 8. For the high-speed output

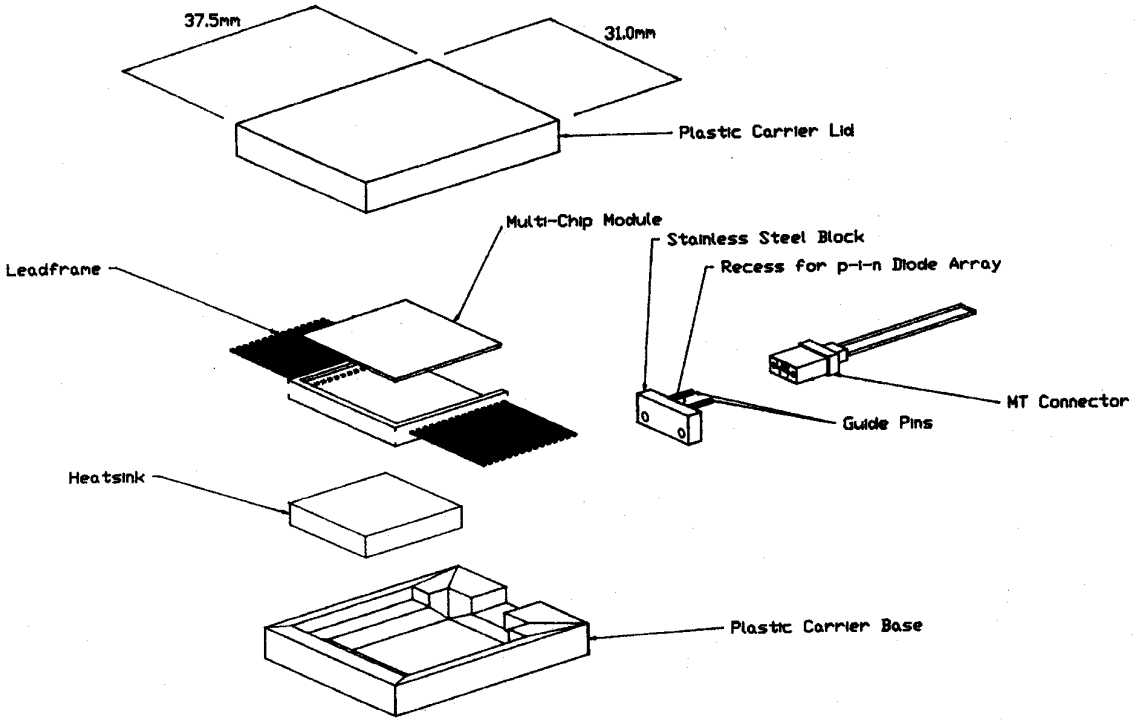


Fig. 7. Illustration of the parts constituting the hybrid receiver array module.

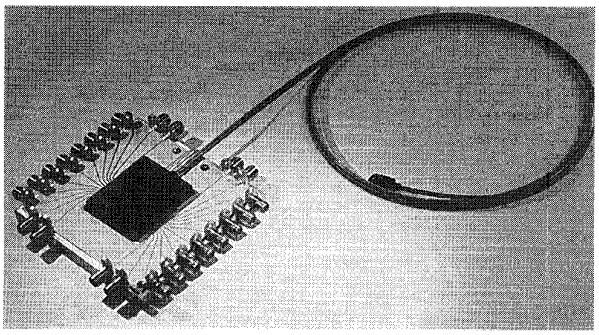

Fig. 8. Photograph of the receiver array module mounted on evaluation board for digital measurements.

signals, an RT-Duroid substrate patterned with 50-Ω microstrip transmission lines was utilized. The evaluation board mounted on a brass block carrying coaxial cable connectors measures 79 mm × 83 mm. Each of the optical transmitters used in evaluating the receiver array module consists of a low-threshold strained InGaAs/GaAs single quantum well laser diode with monolithically integrated intracavity modulators. These voltage-controlled devices operate at 980 nm and enable on–off digital modulation at 1.5 Gb/s [11]. Low skew 12-channel 62.5/125 $\mu$m graded-index MM optical ribbon fiber [18] connectorized with plastic-molded MT connectors was utilized.

The coupling efficiency between the fiber ribbon and the photodiode array for the 12 channels was measured to be 78% ± 5%. The overall crosstalk was measured using an analog version of the receiver (i.e., without the D-register chips) and was found to be less than −40 dB at clock frequencies

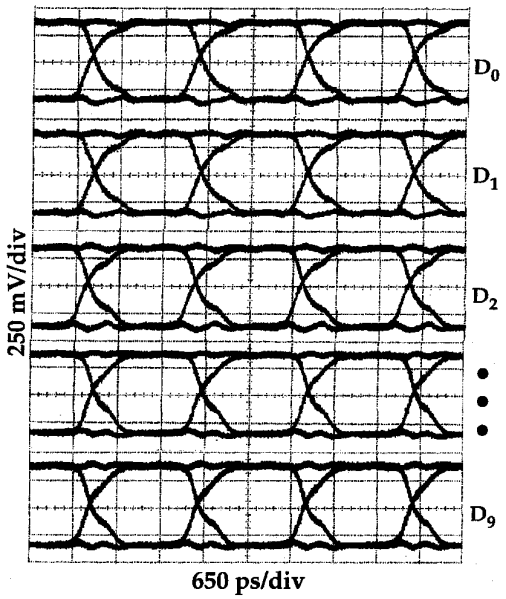


Fig. 9. Retimed synchronous output eye-diagrams of the data channels at 622 Mb/s.

up to 1 GHz [17]. The eye-diagrams of the data channels for a 622 Mb/s $2^7 - 1$ pseudo-random bit stream (PRBS) synchronous transmission are shown in Fig. 9. The clock-to-data phase-margin versus the clock frequency was measured at an eye-edge threshold of $10^{-7}$ and is shown in Fig. 10. A phase margin of 330 °C is obtained at the clock rate of 622 MHz. In Fig. 11, we show the measured BER as a function of the received optical input power using a $2^7 - 1$ PRBS

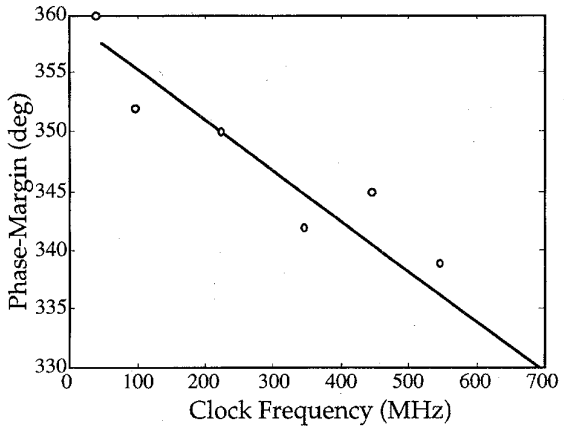


Fig. 10. Output signal phase margin versus transmitted clock frequency measured at an eye-edge threshold of $10^{-7}$.

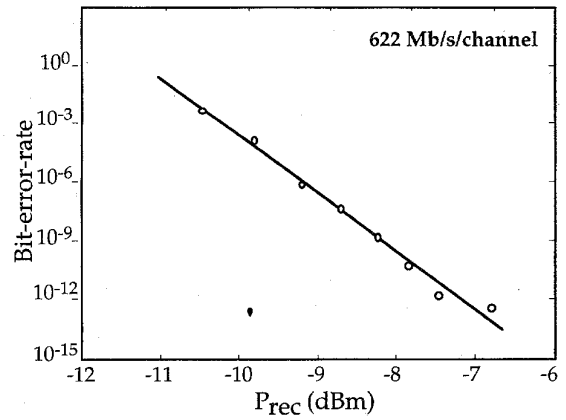


Fig. 11. Measured BER versus received optical power at 622 Mb/s.

at 622 Mb/s. A BER floor of $\sim 5 \times 10^{-13}$ caused by burst-errors is observed. The origin of these burst-errors is presently not known and does not seem to be caused by the TIAA interchannel crosstalk. Note that the received power levels in Fig. 11 are much greater than the Gaussian noise-limited sensitivity of the TIA due to the large decision threshold ambiguity widths of the decision circuits for single-ended input signals. The synchronous operation bandwidth of the receiver module was limited by the commercial flip-flops to 700 MHz.

## V. Future Work

In the next generation of receivers, faster decision circuits will be designed to extend the operating bandwidth per channel to >1 Gb/s. Efforts will be taken to integrate the analog front-end amplifiers and the decision circuits monolithically to reduce package parasitics at the interfaces of the sub-circuits. Additional functionality in the form of multiplexers/demultiplexers may be added to build optical communication LSI's. The improved accuracies of passive alignment techniques and polymer waveguides would promote the monolithic integration of photodetectors. At the package level, reduction of module footprint can be effected through the use of pin grid arrays (PGA's). A hinged clip may be developed to lock the MT connector while a safety mechanism needs to be built at the circuit level to switch the transmitter off when the MT-connector is disconnected.

## VI. Conclusion

We have demonstrated a 12 × 622 Mb/s receiver module for parallel optical digital links using hybrid packaging. Fixturing is used to provide passive alignment between the photodiode array and the MT-connector of a ribbon fiber. The receiver operates synchronously at 622 Mb/s/channel with $<-40$ dB inter-channel crosstalk and 330° phase margin.

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